Docket No.
87552.99R134/SE-906D

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant	:	Linn et al.	)	
			)	
Serial No.	:	09/316,580	)	Examiner:
			)	S. Loke
Filed	:	May 21, 1999	)	
			)	
For	:	BONDED WAFER WITH METAL SILICIDATION	)	Art Unit:
			)	2811
			)	
			)	

APPEAL UNDER 37 CFR §1.191

Table of Contents

Docket No.
87552.99R134/SE-906D

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant	:	Linn et al.	
Serial No.	:	09/316,580	Examiner: S. Loke
Filed	:	May 21, 1999	
For	:	BONDED WAFER WITH METAL SILICIDATION	Art Unit: 2811

APPEAL UNDER 37 CFR §1.191

Assistant Commissioner for Patents
Washington, D.C. 20231
Box **AF**

Sir:

Having filed a Notice of Appeal on April 6, 2000, appellants hereby submit their Appeal Brief in triplicate.

Real Party in Interest

The real party in interest is the Assignee, Intersil Corporation, 1025 West NASA Boulevard, Melbourne, Florida.

Related Appeals and Interferences

There are no related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims

Claims 1-5, 7-11, and 13-22 have been finally rejected under 35 U.S.C. §112, first paragraph, as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claims 10, 11, and 13-22 have been finally rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the applicants regard as the invention.

Claims 1-4 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi, U.S. Patent No. 5,102,821 ("Moslehi"), in view of See et al., U.S. Patent No. 5,212,397 ("See").

Claim 5 has been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi, in view of See, and further in view of Sugimoto et al., JP 02-206118 ("Sugimoto").

Claims 10, 11, 13, 14, 16, and 19-22 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi, in view of See, and further in view of Iwamatsu., JP 02-18961 ("Iwamatsu").

Claims 15 and 17 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi, in view of See, and further in view of Iwamatsu and Sugimoto.

Claims 7-9 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Ochiai, U.S. Patent No. 5,378,919 ("Ochiai") in view of Kameyama et al., JP 01-73659 ("Kameyama").

Claims 10, 16, and 18 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Ochiai in view of Kameyama, and further in view of Iwamatsu.

Status of Amendments

14, 15, 18

In an Amendment filed November 2, 1999, claims 1, 7, 10, 11, 13, and 17 were amended, claims 6 and 12 were canceled, and new claims 19-22 were added.

In an Amendment under 37 CFR §1.116 filed March 6, 2000, the applicants requested the amendment of claims 4 and 5 and the further amendment of claims 10, 11, and 13. In an Advisory Action mailed March 21, 2000, it was asserted that the proposed amendments raised new issues and would not be entered, even upon the filing of an appeal.

Summary of Invention

Claims 1-5 are directed to a silicon-on-insulator integrated circuit that comprises a handle die, a substantially continuous and [unbroken] silicide layer over the handle die, a substantially continuous and [unbroken] first dielectric layer that overlies one side of the [first dielectric] silicide layer, a second dielectric layer on the handle die that underlies the opposite side of the silicide layer, a device silicon layer that overlies the first dielectric layer, and interconnected transistors disposed in and at an upper surface of the device silicon layer.

figs. 3d-3g

Claims 7-9 are directed to a silicon-on-insulator integrated circuit that comprises a handle die, a first dielectric layer formed on the handle die, a substantially continuous and [unbroken] silicide layer having a controlled resistance that is formed on the first dielectric layer and provides a diffusion barrier to impurities, a substantially continuous and [unbroken] second dielectric layer disposed between the silicide layer and a device silicon layer, trenches extending through the device silicon and silicide layers and separating the device silicon [lyer] layer into islands each with an underlying continuous silicide area, and interconnected transistors disposed in and at an upper surface of the device silicon layer.

figs. 4b-4d

Claims 10-22 are directed to a bonded wafer integrated circuit that comprises a handle die comprising a first dielectric layer that includes [a] first bonding material, a silicide layer bonded by the first bonding material to the first dielectric layer, a device wafer comprising a device layer and a second dielectric layer that includes a second bonding material, [and] interconnected transistors in and at a surface of the device layer.

not OK

figs. 5a-5b

The second dielectric layer is bonded to the silicide layer and device layer by the second bonding material, and the silicide layer includes a third bonding material that bonds the silicide layer to the handle die and the device wafer.

Claims 1-5, 7-11, and 13-22 read on the specification and figures as follows:

Claim		Reference to Specification and Figures
1		page 3, lines 23-28; FIGS. 3a-g
2		page 4, lines 12-18; page 7, lines 11-12; page 12, lines 9-10
3		page 6, lines 12-22;FIGS. 3e-f
4	not OK	page 7, lines 2-7; FIG. 3g
5		page 5, lines 10-13; page 7,lines 10-11
7		page 3, line 29 to page 4, line 5; FIGS. 4a-d
8		page 8, lines 17-20; FIGS. 4c-d
9		page 8, lines 28-30; FIG. 4d
10		page 4, lines 6-11; FIGS. 5a-b
11	not OK	page 11, lines 11-16; FIG. 6
13		page 9, lines 7-13
14		page 4, lines 12-18; page 7, lines 11-12; page 12, lines 9-10
15	not OK	page 11, lines 2-16; FIG. 6
16		page 11, lines 10-11; FIG. 6
17		page 11, lines 2-10; FIG. 6
18		page 8, lines 17-20; FIG. 4c
19		page 5, lines 14-31; FIGS. 3a-b not OK
20		page 9, lines 15-21; FIG. 5a
21		page 9, lines 15-17
22		page 10, lines 28-32

Issues

The issues in this appeal are:

the propriety of the final rejection of claims 1-5, 7-11, and 13-22 under 35 U.S.C. §112, first paragraph

the propriety of the final rejection of claims 10, 11, and 13-22 under 35 U.S.C. §112, second paragraph

the propriety of the final rejection of claims 1-4 under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See

the propriety of the final rejection of claim 5 under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See, and further in view of Sugimoto

the propriety of the final rejection of claims 10, 11, 13, 14, 16, and 19-22 under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See, and further in view of Iwamatsu

the propriety of the final rejection of claims 15 and 17 under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See, and further in view of Iwamatsu and Sugimoto

the propriety of the final rejection of claims 7-9 under 35 U.S.C. §103(a) as being unpatentable over Ochiai in view of Kameyama

the propriety of the final rejection of claims 10, 16, and 18 under 35 U.S.C. §103(a) as being unpatentable over Ochiai in view of Kameyama, and further in view of Iwamatsu.

Grouping of Claims

Claims 1-5 stand or fall together.

Claims 7-9 stand or fall together.

Claims 10-11, 13-15, and 22 stand or fall together.

Claims 16-18 stand or fall together.

Claims 19-21 stand or fall together.

Argument

In the Office Action mailed January 6, 2000, the specification and abstract of the instant continuation application, filed May 21, 1999, were again objected to under U.S.C. §132 on the grounds that they introduced new matter not supported by the disclosure of the original parent application. Relatedly, claims 1-5, 7-11, and 13-22 were finally rejected under 35 U.S.C. §112, first paragraph, and claims 10-11 and 13-22 were finally rejected under 35 U.S.C. §112, second paragraph.

The appellants' Amendment under 37 CFR §1.116, in response to the §112, second paragraph, rejection of claims 10-11 and 13-22, offered clarifying amendments of claims 10 and 13. With regard to claim 10, it was proposed that the claim be reworded at lines 10-11 to describe more clearly the bonding of the silicide layer to the handle die and device wafer by a third bonding material. With regard to claim 13, the proposed amendment was simply to insert, at line 2, an open bracket before "portion" that had been inadvertently omitted in the previous amendment of this claim, filed November 2, 1999, which did include the close bracket after "layer." In an Advisory Action, whose mailing date was shown as March 21, 2000 but was not received in the office of the appellants' attorney until April 7, 2000 (a day after the deadline for filing a Notice of Appeal), the appellants were informed that these proposed amendments would not be entered.

In the Remarks section of the Amendment filed November 2, 1999 and reiterated in the Amendment under 37 CFR §1.116 filed March 6, 2000, the applicants, in responding to the assertion that the original specification does not disclose interconnected transistors in and at the surface of the device silicon layer, as claimed in claims 1, 7, and 10, directed the Examiner's attention to FIG. 3g and its description at page 7, lines 5-7, of the instant specification: "FIG. 3g schematically shows in expanded cross-sectional elevation view a partially completed MOSFET in island 322, which would be just one of thousands of such devices in an integrated circuit fabricated on the bonded wafer." (Emphasis added) Clearly, the MOSFET depicted in FIG. 3g is located in and at the surface of device silicon layer 322, and, as one of many transistors included in an integrated circuit, would be connected with

other transistors in the circuit. The Examiner has continued to maintain that the original specification does not disclose that these MOSFETs are connected with other transistors in the circuit. However, the original specification states that the present invention relates to electronic integrated circuits and dielectrically isolated integrated circuits. By definition, the devices included in an integrated circuit are interconnected, i.e., connected with one another. Therefore the references to interconnected transistors at page 3, line 28, page 4, lines 4-5, and page 8, line 32 to page 9, line 2, in the specification and at page 16, lines 7-8, 15-16, and 18 in the abstract, being fully supported in the original disclosure, introduce no new matter.

In response to the Examiner's objection to the sentence "The silicide layer...the silicide layer." at page 4, lines 9-11 of the specification, which is repeated in the abstract at page 26, lines 18-21 and also provides the basis for the more detailed description included in claim 10, the appellants have respectfully called attention to the description of FIGS. 5a-b on page 9, lines 5-21, which was present in the original specification. Handle die (512) comprises a first dielectric layer (oxide layer 513) that comprises a first bonding material (polysilicon 514) that bonds a silicide layer (WSi_2 515 formed from tungsten 518) to the first dielectric layer. Device wafer (502) includes a second dielectric layer (oxide layer 506) that comprises a second bonding material (polysilicon 517) that bonds the silicide layer to the second dielectric layer. A third bonding material (aqueous solution of HNO_3 and H_2O_2 505) bonds the silicide layer to the handle die and the device wafer via the dielectric layers. It is clear, therefore, that no new matter is introduced into the disclosure by the cited sentence in the specification and abstract.

Claims 1-4 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See et al. Claim 5 has been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See et al. and further in view of Sugimoto et al. Also claims 10, 11, 13, 14, 16, and 19-22 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See et al. and further in view of Iwamatsu. Claims 15 and 17 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See et al. and further in view of Iwamatsu and Sugimoto et al.

Throughout the prosecution of both the parent application and the instant continuation application, the Examiner has persistently maintained that substantial similarity exists between the bonded structure of the present invention, one embodiment of which is depicted in Figures 4a-d, and the SOI wafer of Moslehi, represented in Figures 2a-f of the reference. A comparison of these sets of figures and their respective supporting disclosures, however, makes it readily apparent how grossly dissimilar are the appellants' and the Moslehi structures.

As depicted in Figure 4b of the instant application, a continuous, unpatterned layer 415 of $CoSi_2$ overlies handle oxide layer 413. Figure 4c illustrates trenches extending through the silicide layer to form islands, each with an underlying continuous silicide area. The Moslehi structure, on the other hand, includes, as shown in Figures 2e-f, a layer containing both a silicide (40) and a metal (e.g., titanium 24) in a grid pattern over oxide layer 22. The Examiner's persistent characterization of the silicide grid of Moslehi as a continuous layer is incomprehensible to the appellants.

The integrated circuit of the present invention and the Moslehi structure can also be differentiated in several other important respects. In the present invention, the silicide layer 415 lies between and is thereby adjacent to both first and second dielectric (oxide) layers 406 and 413, respectively, as shown in Figures 4b-d. The thin (500 angstroms thick, cf. page 7, lines 25-31) unpatterned polysilicon layers 417 and 414 shown in Figure 4(a) are substantially completely consumed in the reaction with Co to form silicide layer 415. In the Moslehi structure, by contrast, the grid-patterned layer containing silicide (40) and metal (24) is adjacent to a single oxide layer 22 and overlies a corresponding grid pattern of relatively thick (2 μm, cf. column 3, lines 22-23) polysilicon 38 and micro-vacuum chambers 42, an essential feature of the reference that is absent in the appellants' integrated circuit. The oxide layer 36 is spaced from the silicide layer 40 by the residual polysilicon 38.

The silicide layer 415 of the present invention constitutes a diffusion barrier to impurities. In the January 6, 2000 Office Action at page 7, third paragraph, the Examiner stated that it is well known in the art that a metal silicide layer (emphasis added) can prevent diffusion of harmful ions into the device layer. However the

metal-metal silicide grid structure of Moslehi, which exposes the copper wafer to contaminants, is clearly deficient as a diffusion barrier, as evidenced by the disclosure of and claims to an additional separate diffusion resistant layer of nitride adjacent to an oxide layer (cf. column 2, lines 28-30, claims 3-4). The continuous silicide layer of the present invention, by contrast, serves both as a bonding layer and as a diffusion barrier, no separate barrier layer being required.

See et al. is relied on for its teaching of bipolar and MOS transistors formed on a silicon substrate. At page 7, third paragraph, of the January 6, 2000 Office Action, the Examiner asserted that the "combination of Moslehi and See et al. shows all the required elements of the claimed invention." Given the several major discrepancies between the teachings of Moslehi and the present invention, as emphasized in the preceding discussion, this assertion is clearly untenable. Similarly untenable is the Examiner's further assertion in the same paragraph that the combination of the Moslehi and See et al. disclosures with that of Sugimoto et al., which is relied on solely for its disclosure of a diamond dielectric layer, "shows the required element of the dependent claim."

Iwamatsu teaches implantation at about three million electron volts of ions of Si, O, N, H, P, B, As, etc, into a silicon film disposed on a silicon dioxide layer that had been previously bonded to a second silicon dioxide layer and asserts that maximum ion formation occurs at the interface of the bonded silicon dioxide layers. In the Office Actions, the Examiner has attempted to combine this disclosure of Iwamatsu with the teachings of Moslehi and the other cited references in finding claims 10-11, 13-17, and 19-22 unpatentable, an attempt that is not only improper but also unclear as to its intent.

In regard to instant claims 19-21, which recite first and second bonding materials each comprising a thin layer of polysilicon that is substantially consumed during bonding, and further recites that the first bonding material includes an aqueous oxidizing solution that can comprise nitric acid and hydrogen peroxide, the appellants respectfully note that none of the cited references teach such bonding materials.

Claims 7-9 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Ochiai, in view of Kameyama et al. Also, claims 10, 16, and 18

have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Ochiai in view of Kameyama et al. and further in view of Iwamatsu.

Ochiai discloses an integrated circuit device with an SOI structure and comprising a plurality of transistors, each overlying an insulating layer [55] disposed above a resistance layer [52] that is buried in a crevice [61] in a second insulating layer [51]. The Ochiai semiconductor structure is a "sea-of-gate array" and thus includes no trenches to define device islands. By contrast, claims 7-9 and 16-18 of the instant application require trenches. In both the August 3, 1999 and January 6, 2000 Office Actions, the Examiner implicitly acknowledged this lack of disclosure of trenches in the reference with the ambiguous and unsupported assertion that "The insulating region between the transistors can be considered as the trench." (emphasis added).

Also, as was acknowledged in the August 3, 1999 Office Action, Ochiai does not show a resistance layer made of silicide. In fact, Ochiai makes no mention whatsoever of silicides. Kameyama discloses a patterned polycrystalline tungsten silicide resistor thin film formed between two oxide layers and having aluminum electrodes connected at both ends. By contrast, instant claim 7 recites that the silicide layer is "substantially continuous and unbroken...,...providing a diffusion barrier to impurities".

In ¶10 on page 6 of the January 6, 2000 Office Action, the Examiner acknowledged that "Ochiai differs from the claimed invention by not showing a bonding material includes nitrogen material" but then went on to cite Iwamatsu as showing that nitrogen can be implanted in a silicon dioxide layer. The disclosure of Iwamatsu with respect to the appellants' invention is no more properly combinable with the teachings of Ochiai and Kameyamaha than it is with Moslehi.

In the second paragraph on page 7 of the January 6, 2000 Office Action, the Examiner observed that "fig. 6 shows the buried layer of claim 4 and the diamond layer of claim 5" and then raises the objection that "claims 4 and 5 are depending to claim 1 which discloses the device of figs. 3f and 3g. Neither fig.3f nor fig. 3g discloses the buried layer and the diamond layer." The appellants respectfully point out that the patent laws, rules, and MPEP provide no basis for such an objection or

rejection. No authority is cited, nor can any be cited, for the Examiner's position that a claim is unpatentable because no one figure shows all the features of the claim. Disclosure within the specification of the invention to which the claim is directed is sufficient.

not OK

Conclusion

The foregoing discussion makes clear that:

the final rejection of claims 1-5, 7-11, and 13-22 under 35 U.S.C. §112, first paragraph, is improper

the final rejection of claims 10, 11, and 13-22 under 35 U.S.C. §112, second paragraph, is improper

the final rejection of claims 1-4 under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See is improper

the final rejection of claim 5 under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See, and further in view of Sugimoto is improper

the final rejection of claims 10, 11, 13, 14, 16, and 19-22 under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See, and further in view of Iwamatsu is improper

the final rejection of claims 15 and 17 under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See, and further in view of Iwamatsu and Sugimoto is improper

the final rejection of claims 7-9 under 35 U.S.C. §103(a) as being unpatentable over Ochiai in view of Kameyama is improper

the final rejection of claims 10, 16, and 18 under 35 U.S.C. §103(a) as being unpatentable over Ochiai in view of Kameyama, and further in view of Iwamatsu is improper.

The appellants therefore respectfully request that the final rejection of claims 1-5, 7-11, and 13-22 be reversed and all of these claims allowed.

Respectfully submitted,

July 5, 2000
Date

Lee J. Fleckenstein
Lee J. Fleckenstein
Registration No. 36,136

JAECKLE FLEISCHMANN & MUGEL, LLP
39 State Street
Rochester, New York 14614-1310
Telephone: (716) 262-0950
Facsimile: (716) 262-4133

Appendix

Claims 1-5, 7-11, 13-22:

1. A silicon-on-insulator integrated circuit, comprising:

(a) a handle die;

(b) a substantially continuous and unbroken silicide layer over said handle die,

(c) a substantially continuous and unbroken first dielectric layer overlying one side of said silicide layer;

(d) a device silicon layer overlying said first dielectric layer, said device silicon layer having an upper surface;

(e) a second dielectric layer on said handle die underlying the opposite side of said silicide layer; and

(f) interconnected transistors in and at the upper surface of said device silicon layer.

2. The integrated circuit of claim 1 wherein said silicide layer comprises a diffusion barrier to impurities.

3. The integrated circuit of claim 1 further comprising:

(g) trenches extending through said device silicon layer and separating said device silicon layer into islands.

4. The integrated circuit of claim 1 wherein said device silicon layer includes deep buried layers abutting said dielectric layer.

5. The integrated circuit of claim 1 wherein said handle wafer comprises silicon and at least one of said dielectric layers comprises diamond.

7. A silicon-on insulator integrated circuit comprising:

(a) a handle die;

(b) a first dielectric layer formed on said handle die

(c) a substantially continuous and unbroken silicide layer formed on said first dielectric layer, said silicide layer having a controlled resistance and providing a diffusion barrier to impurities;

(d) a substantially continuous and unbroken second dielectric layer disposed between said silicide layer and a device silicon layer;

(e) trenches extending through said device silicon layer and silicide layer and separating said device silicon layer into islands each with an underlying continuous silicide area; and

(f) interconnected transistors in and at an upper surface of said device silicon layer.

8. The integrated circuit of claim 7 further comprising:

(g) trenches extending through at least one of said islands to said underlying silicide area, said trenches having dielectric sidewalls and containing conductive material in contact with said silicide area.

9. The integrated circuit of claim 8 wherein said islands have a thickness no greater than about 2 μm, and said conductive material is tungsten.

10. A bonded wafer integrated circuit comprising:

(a) a handle die comprising a first dielectric layer, said first dielectric layer comprising a first bonding material;

(b) a silicide layer bonded by said first bonding material to said first dielectric layer;

(c) a device wafer comprising a device layer and a second dielectric layer comprising a [[a]] second bonding material, said second dielectric layer being bonded to said silicide layer and said device layer by said second bonding material; and

(d) interconnected transistors in and at a surface of said device layer;

wherein said silicide layer comprises a third bonding material that bonds said silicide layer to said handle die and said device wafer.

11. The integrated circuit of claim 10 wherein said device layer is silicon and includes doped buried layers abutting said silicide layer and forming components of said transistors.

13. The integrated circuit of claim 10 wherein said handle die is silicon and said first dielectric layer is silicon dioxide portion adjacent said homogeneous silicide layer].

14. The integrated circuit of claim 10 wherein said homogeneous silicide layer comprises a diffusion barrier to impurities.

15. The integrated circuit of claim 10 wherein said device includes a layer of diamond adjacent said homogeneous silicide layer and a layer of silicon adjacent said diamond layer, said transistors being formed in and at a surface of said silicon layer.

16. The integrated circuit of claim 10 further comprising:

(e) trenches extending into said device layer and separating a semiconductor layer of said device layer into islands that isolate each of said transistors.

17. The integrated circuit of claim 16 wherein said device layer includes a diamond layer adjacent to said homogeneous silicide layer, said trenches extending to but not through said diamond layer.

18. The integrated circuit of claim 16 wherein said homogeneous silicide layer is conductive, said trenches extend through said silicide layer to separate said silicide layer into buried layers between said islands and said handle die, and electrical contacts extend through said device layer to said buried layers.

19. The integrated circuit of claim 10 wherein said first and second bonding materials each comprises a thin layer of polysilicon, said polysilicon being substantially consumed during bonding.

20. The integrated circuit of claim 19 wherein said first bonding material further comprises an aqueous oxidizing solution.

21. The integrated circuit of claim 20 wherein said aqueous oxidizing solution comprises nitric acid and hydrogen peroxide.

22. The integrated circuit of claim 10 wherein said third bonding material is a silicide of a metal selected from the group consisting of cobalt, platinum, tungsten, and titanium.